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Authors

B. Abi,[129] R. Acciarri,[56] Mario A. Acero,[8] G. Adamov,[59] D. Adams,[15] M. Adinolfi,[14] Z. Ahmad,[163] J. Ahmed,[166] T. Alion,[153] S. Alonso Monsalve,[18] C. Alt,[49] J. Anderson,[4] C. Andreopoulos,[109] M. P. Andrews,[56] F. Andrianala,[2] S. Andringa,[103] A. Ankowski,[143] J. Anthony,[28] M. Antonova,[72] S. Antusch,[9] A. Aranda Fernandez,[36] A. Ariga,[10] L. O. Arnold,[39] M. A. Arroyave,[48] J. Asaadi,[157] A. Aurisano,[34] V. Aushev,[101] D. Autiero,[81] F. Azfar,[129] H. Back,[130] J. J. Back,[166] C. Backhouse,[161] P. Baesso,[14] L. Bagby,[56] R. Bajou,[1] S. Balasubramanian,[170] P. Baldi,[23] B. Bambah,[70] F. Barao,[103, 105] G. Barenboim,[72] G. J. Barker,[166] W. Barkhouse,[123] C. Barnes,[116] G. Barr,[129] J. Barranco Monarca,[64] N. Barros,[103, 106] J. L. Barrow,[155, 56] A. Bashyal,[128] V. Basque,[114] F. Bay,[122] J. L. Bazo Alba,[137] J. F. Beacom,[127] E. Bechetoille,[81] B. Behera,[38] L. Bellantoni,[56] G. Bellettini,[135] V. Bellini,[74] O. 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Gnani,[108] O. Gogota,[101] M. Gold,[120] S. Gollapinni,[110] K. Gollwitzer,[56] R. A. Gomes,[52] L. V. Gomez Bermeo,[145] L. S. Gomez Fajardo,[145] F. Gonnella,[12] J. A. Gonzalez-Cuevas,[6] M. C. Goodman,[4] O. Goodwin,[114] S. Goswami,[134] C. Gotti,[76] E. Goudzovski,[12] C. Grace,[108] M. Graham,[143] E. Gramellini,[170] R. Gran,[118] E. Granados,[64] A. Grant,[44] C. Grant,[13] D. Gratieri,[58] P. Green,[114] S. Green,[28] L. Greenler,[169] M. Greenwood,[128] J. Greer,[14] W. C. Griffith,[153] M. Groh,[88] J. Grudzinski,[4] K. Grzelak,[165] W. Gu,[15] V. Guarino,[4] R. Guenette,[67] A. Guglielmi,[131] B. Guo,[149] K. K. Guthikonda,[65] R. Gutierrez,[3] P. Guzowski,[114] M. M. Guzzo,[29] S. Gwon,[33] A. Habig,[118] A. Hackenburg,[170] H. Hadavand,[157] R. Haenni,[10] A. Hahn,[56] J. Haigh,[166] J. Haiston,[147] T. Hamernik,[56] P. Hamilton,[85] J. Han,[136] K. Harder,[142] D. A. Harris,[172, 56] J. Hartnell,[153] T. Hasegawa,[96] R. Hatcher,[56] E. Hazen,[13] A. Heavey,[56] K. M. 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A. Izmaylov,[72] E. James,[56] B. Jargowsky,[23] F. Jediny,[41] C. Jesús-Valls,[71] X. Ji,[15] L. Jiang,[164] S. Jiménez,[19] A. Jipa,[16] A. Joglekar,[25] C. Johnson,[38] R. Johnson,[34] B. Jones,[157] S. Jones,[161] C. K. Jung,[151] T. Junk,[56] Y. Jwa,[39] M. Kabirnezhad,[129] A. Kaboth,[142] I. Kadenko,[101] F. Kamiya,[54] G. Karagiorgi,[39] A. Karcher,[108] M. Karolak,[17] Y. Karyotakis,[20] S. Kasai,[100] S. P. Kasetti,[111] L. Kashur,[38] N. Kazaryan,[171] E. Kearns,[13] P. Keener,[132] K.J. Kelly,[56] E. Kemp,[29] W. Ketchum,[56] S. H. Kettell,[15] M. Khabibullin,[80] A. Khotjantsev,[80] A. Khvedelidze,[59] D. Kim,[18] B. King,[56] B. Kirby,[15] M. Kirby,[56] J. Klein,[132] K. Koehler,[169] L. W. Koerner,[69] S. Kohn,[21,108] P. P. Koller,[10] M. Kordosky,[168] T. Kosc,[81] U. Kose,[18] V. A. Kostelecký,[88] K. Kothekar,[14] F. Krennrich,[91] I. Kreslo,[10] Y. Kudenko,[80] V. A. Kudryavtsev,[146] S. Kulagin,[80] J. Kumar,[68] R. Kumar,[139] C. Kuruppu,[149] V. Kus,[41] T. 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T. Schaffer,[118] H. Schellman,[128,56] P. Schlabach,[56] D. Schmitz,[32] K. Scholberg,[46] A. Schukraft,[56] E. Segreto,[29] J. Sensenig,[132] I. Seong,[23] A. Sergi,[12] F. Sergiampietri,[151] D. Sgalaberna,[18] M. H. Shaevitz,[39] S. Shafaq,[94] M. Shamma,[25] H. R. Sharma,[93] R. Sharma,[15] T. Shaw,[56] C. Shepherd-Themistocleous,[142] S. Shin,[32] D. Shooltz,[117] R. Shrock,[151] L. Simard,[102] N. Simos,[15] J. Sinclair,[10] G. Sinev,[46] J. Singh,[112] J. Singh,[112] R. Sipos,[18] F. W. Sippach,[39] G. Sirri,[73] A. Sitraka,[147] K. Siyeon,[33] D. Smargianaki,[151] A. Smith,[46] A. Smith,[28] E. Smith,[88] P. Smith,[88] J. Smolik,[41] M. Smy,[23] P. Snopok,[84] M. Soares Nunes,[29] H. Sobel,[23] M. Soderberg,[154] C. J. Solano Salinas,[89] S. Söldner-Rembold,[114] N. Solomey,[167] V. Solovov,[104] W. E. Sondheim,[110] M. Sorel,[72] J. Soto-Oton,[19] A. Sousa,[34] K. Soustruznik,[31] F. Spagliardi,[129] M. Spanu,[15] J. Spitz,[116] N. J. Spooner,[146] K. Spurgeon,[154] R. Staley,[12] M. Stancari,[56] L. Stanco,[131] H. M. Steiner,[108] J. Stewart,[15] B. Stillwell,[32] J. Stock,[147] F. Stocker,[18] T. Stokes,[111] M. Strait,[160] T. Strauss,[56] S. Striganov,[56] A. Stuart,[36] D. Summers,[119] A. Surdo,[144] V. Susic,[9] L. Suter,[56] C. M. Sutera,[74] R. Svoboda,[22] B. Szczerbinska,[156] A. Szelc,[114] R. Talaga,[4] H. A. Tanaka,[143] B. Tapia Oregui,[158] A. Tapper,[85] S. Tariq,[56] E. Tatar,[83] R. Tayloe,[88] A. M. Teklu,[151] M. Tenti,[73] K. Terao,[143] C. A. Ternes,[72] F. Terranova,[76] G. Testera,[75] A. Thea,[142] J. L. Thompson,[146] C. Thorn,[15] S. C. Timm,[56] A. Tonazzo,[1] M. Torti,[76] M. Tortola,[72] F. Tortorici,[74] D. Totani,[56] M. Toups,[56] C. Touramanis,[109] J. Trevor,[27] W. H. Trzaska,[95] Y. T. Tsai,[143] Z. Tsamalaidze,[59] K. V. Tsang,[143] N. Tsverava,[59] S. Tufanli,[18] C. Tull,[108] E. Tyley,[146] M. Tzanov,[111] M. A. Uchida,[28] J. Urheim,[88] T. Usher,[143] M. R. Vagins,[99] P. Vahle,[168] G. A. Valdiviesso,[51] E. Valencia,[168] Z. Vallari,[27] J. W. F. Valle,[72] S. Vallecorsa,[18] R. Van Berg,[132] R. G. Van de Water,[110] D. Vanegas Forero,[29] F. Varanini,[131] D. Vargas,[71] G. Varner,[68] J. Vasel,[88] G. Vasseur,[17] K. Vaziri,[56] S. Ventura,[131] A. Verdugo,[19] S. Vergani,[28] M. A. Vermeulen,[122] M. Verzocchi,[56] H. Vieira de Souza,[29] C. Vignoli,[61] C. Vilela,[151] B. Viren,[15] T. Vrba,[41] T. Wachala,[121] A. V. Waldron,[85] M. Wallbank,[34] H. Wang,[24] J. Wang,[22] Y. Wang,[24] Y. Wang,[151] K. Warburton,[91] D. Warner,[38] M. Wascko,[85] D. Waters,[161] A. Watson,[12] P. Weatherly,[45] A. Weber,[142,129] M. Weber,[10] H. Wei,[15] A. Weinstein,[91] D. Wenman,[169] M. Wetstein,[91] M. R. While,[147] A. White,[157] L. H. Whitehead,[28] D. Whittington,[154] M. J. Wilking,[151] C. Wilkinson,[10] Z. Williams,[157] F. Wilson,[142] R. J. Wilson,[38] J. Wolcott,[159] T. Wongjirad,[159] K. Wood,[151] L. Wood,[130] E. Worcester,[15] M. Worcester,[15] C. Wret,[140] W. Wu,[56] W. Wu,[23] Y. Xiao,[23] G. Yang,[151] T. Yang,[56] N. Yershov,[80] K. Yonehara,[56] T. Young,[123] B. Yu,[15] J. Yu,[157] J. Zalesak,[40] L. Zambelli,[20] B. Zamorano,[62] A. Zani,[77] L. Zazueta,[168] G. P. Zeller,[56] J. Zennamo,[56] K. Zeug,[169] C. Zhang,[15] M. Zhao,[15] E. Zhivun,[15] G. Zhu,[127] E. D. Zimmerman,[37] M. Zito,[17] S. Zucchelli,[73] J. Zuklin,[40] V. Zutshi,[124] and R. Zwaska[56]

(The DUNE Collaboration)

[1] *APC - Université de Paris, CNRS/IN2P3, CEA/lrfu, Observatoire de Paris, 10, rue Alice Domon et Léonie Duquet, 75205 Paris Cedex 13, France*
[2] *University of Antananarivo, BP 566, Antananarivo 101, Madagascar*
[3] *Universidad Antonio Nariño, Cra 3 Este No 47A-15, Bogotá, Colombia*
[4] *Argonne National Laboratory, Argonne, IL 60439, USA*
[5] *University of Arizona, 1118 E. Fourth Street Tucson, AZ 85721, USA*
[6] *Universidad Nacional de Asunción, San Lorenzo, Paraguay*
[7] *University of Athens, University Campus, Zografou GR 157 84, Greece*
[8] *Universidad del Atlantico, Carrera 30 Número 8- 49 Puerto Colombia - Atlántico, Colombia*
[9] *University of Basel, Klingelbergstrasse 82, CH-4056 Basel, Switzerland*
[10] *University of Bern, Sidlerstrasse 5, CH-3012 Bern, Switzerland*
[11] *Beykent University, Istanbul*
[12] *University of Birmingham, Edgbaston, Birmingham B15 2TT, United Kingdom*
[13] *Boston University, Boston, MA 02215, USA*
[14] *University of Bristol, H. H. Wills Physics Laboratory, Tyndall Avenue Bristol BS8 1TL, United Kingdom*
[15] *Brookhaven National Laboratory, Upton, NY 11973, USA*
[16] *University of Bucharest, Faculty of Physics, Bucharest, Romania*
[17] *CEA/Saclay, IRFU Institut de Recherche sur les Lois Fondamentales de l'Univers, F-91191 Gif-sur-Yvette CEDEX, France*
[18] *CERN, European Organization for Nuclear Research 1211 Genève 23, Switzerland, CERN*
[19] *CIEMAT, Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas, Av. Complutense, 40, E-28040 Madrid, Spain*
[20] *Laboratoire d'Annecy-le-Vieux de Physique des Particules, CNRS/IN2P3 and Université Savoie Mont Blanc, CNRS/IN2P3 and Université Savoie Mont Blanc, 74941 Annecy-le-Vieux, France*
[21] *University of California Berkeley, Berkeley, CA 94720, USA*
[22] *University of California Davis, Davis, CA 95616, USA*
[23] *University of California Irvine, Irvine, CA 92697, USA*
[24] *University of California Los Angeles, Los Angeles, CA 90095, USA*
[25] *University of California Riverside, 900 University Ave, Riverside CA 92521*
[26] *University of California Santa Barbara, Santa Barbara, California 93106 USA*

[27]California Institute of Technology, Pasadena, CA 91125, USA
[28]University of Cambridge, JJ Thomson Avenue, Cambridge CB3 0HE, United Kingdom
[29]Universidade Estadual de Campinas, Campinas - SP, 13083-970, Brazil
[30]Centro Brasileiro de Pesquisas Físicas, Rio de Janeiro, RJ 22290-180, Brazil
[31]Institute of Particle and Nuclear Physics of the Faculty of Mathematics and Physics of the Charles University in Prague, V Holešovičkách 747/2, 180 00 Praha 8-Libeň, Czech Republic
[32]University of Chicago, Chicago, IL 60637, USA
[33]Chung-Ang University, Dongjak-Gu, Seoul 06974, South Korea
[34]University of Cincinnati, Cincinnati, OH 45221, USA
[35]Centro de Investigacion y de Estudios Avanzados del IPN (Cinvestav), Mexico City
[36]Universidad de Colima, 340 Colonia Villa San Sebastian Colima, Colima, Mexico
[37]University of Colorado Boulder, Boulder, CO 80309, USA
[38]Colorado State University, Fort Collins, CO 80523, USA
[39]Columbia University, New York, NY 10027, USA
[40]Institute of Physics, Czech Academy of Sciences, Na Slovance 2, 182 21 Praha 8, Czech Republic
[41]Czech Technical University in Prague, Břehová 78/7, 115 19 Prague 1, Czech Republic
[42]Dakota State University, Madison, SD 57042, USA
[43]University of Dallas, Irving, TX 75062-4736, USA
[44]Daresbury Laboratory, Daresbury Warrington, Cheshire WA4 4AD, United Kingdom
[45]Drexel University, Philadelphia, PA 19104, USA
[46]Duke University, Durham, NC 27708, USA
[47]Durham University, South Road, Durham DH1 3LE, United Kingdom
[48]Universidad EIA, Via José María Córdoba #km 2 + 200, Envigado, Antioquia
[49]ETH Zurich, Institute for Particle Physics, Zurich, Switzerland
[50]University of Edinburgh, Edinburgh EH8 9YL, United Kingdom
[51]Universidade Federal de Alfenas, Poços de Caldas - MG, 37715-400, Brazil
[52]Universidade Federal de Goias, Goiania, GO 74690-900, Brazil
[53]Universidade Federal de São Carlos, Araras - SP, 13604-900, Brazil
[54]Universidade Federal do ABC, Av. dos Estados 5001, Santo André - SP, 09210-580 Brazil
[55]Universidade Federal do Rio de Janeiro, Rio de Janeiro - RJ, 21941-901, Brazil
[56]Fermi National Accelerator Laboratory, Batavia, IL 60510
[57]University of Florida, PO Box 118440 Gainesville, FL 32611-8440, USA
[58]Fluminense Federal University, Rua Miguel de Frias, 9 Icaraí Niterói - RJ, 24220-900, Brazil
[59]Georgian Technical University, 77 Kostava Str. 0160, Tbilisi, Georgia
[60]Gran Sasso Science Institute, Viale Francesco Crispi 7, L'Aquila, Italy
[61]Laboratori Nazionali del Gran Sasso, I-67010 Assergi, AQ, Italy
[62]University of Granada & CAFPE, Campus Fuentenueva (Edif. Mecenas), 18002 Granada, Spain
[63]University Grenoble Alpes, CNRS, Grenoble INP, LPSC-IN2P3, 38000 Grenoble, France
[64]Universidad de Guanajuato, Gto., C.P. 37000, Mexico
[65]Department of Physics, K L E F, Green Fields, Guntur - 522 502, AP, India
[66]Harish-Chandra Research Institute, Jhunsi, Allahabad 211 019, India
[67]Harvard University, 17 Oxford St. Cambridge, MA 02138, USA
[68]University of Hawaii, Honolulu, HI 96822, USA
[69]University of Houston, Houston, TX 77204, USA
[70]University of Hyderabad, Gachibowli, Hyderabad - 500 046, India
[71]Institut de Fìsica d'Altes Energies, Barcelona i.e. Catalan ersitat Autonoma de Barcelona, Campus UAB, Facultat Ciències Nord, 08193 Bellaterra, Barcelona, Spain
[72]Instituto de Fisica Corpuscular, Catedratico Jose Beltran, 2 E-46980 Paterna (Valencia), Spain
[73]Istituto Nazionale di Fisica Nucleare Bologna, 40127 Bologna BO, Italy
[74]Istituto Nazionale di Fisica Nucleare Sezione di Catania, Via Santa Sofia 64, I-95123 Catania, Italy
[75]Università degli studi di Genova, Istituto Nazionale di Fisica Nucleare Genova, 16126 Genova GE, Italy
[76]Istituto Nazionale di Fisica Nucleare Sezione di Milano Bicocca and University of Milano Bicocca, Piazza della Scienza, 3 - I-20126 Milano, Italy
[77]Istituto Nazionale di Fisica Nucleare Milano, I-20133 Milano, Italy
[78]Istituto Nazionale di Fisica Nucleare - Sezione di Napoli, Complesso Universitario di Monte S. Angelo, I-80126 Napoli, Italy
[79]Università degli studi di Pavia, Istituto Nazionale di Fisica Nucleare Sezione di Pavia, I-27100 Pavia, Italy
[80]Institute for Nuclear Research of the Russian Academy of Sciences , prospekt 60-letiya Oktyabrya 7a, Moscow 117312, Russia
[81]Institut de Physique des 2 Infinis de Lyon, Rue E. Fermi 4 69622 Villeurbanne, France
[82]Institute for Research in Fundamental Sciences , Farmanieh St. Tehran, 19538-33511, Iran
[83]Idaho State University, Department of Physics, Pocatello, ID 83209, USA
[84]Illinois Institute of Technology, Chicago, IL 60616, USA
[85]Imperial College of Science Technology and Medicine, Blackett Laboratory Prince Consort Road, London SW7 2BZ, United Kingdom
[86]Indian Institute of Technology Guwahati, Guwahati, 781 039, India

[87]*Indian Institute of Technology Hyderabad, Hyderabad, 502285, India*
[88]*Indiana University, Bloomington, IN 47405, USA*
[89]*Universidad Nacional de Ingeniería, Av. Tupac Amaru 210, Lima 25, Perú*
[90]*University of Iowa, Department of Physics and Astronomy 203 Van Allen Hall Iowa City, IA 52242, USA*
[91]*Iowa State University, Ames, Iowa 50011, USA*
[92]*Iwate University, Morioka, Iwate 020-8551, Japan*
[93]*University of Jammu, Physics Department, JAMMU-180006, India*
[94]*Jawaharlal Nehru University, School of Physical Sciences, New Delhi 110067, India*
[95]*University of Jyvaskyla, P.O. Box 35, FI-40014, Finland*
[96]*High Energy Accelerator Research Organization (KEK), Ibaraki, 305-0801, Japan*
[97]*Korea Institute of Science and Technology Information, Daejeon, 34141, South Korea*
[98]*Kansas State University, Manhattan, KS 66506, USA*
[99]*Kavli Institute for the Physics and Mathematics of the Universe , Kashiwa, Chiba 277-8583, Japan*
[100]*National Institute of Technology, Kure College, Hiroshima, 737-8506, Japan*
[101]*Kyiv National University, 64, 01601 Kyiv, Ukraine*
[102]*Laboratoire de l'Accélérateur Linéaire , Bâtiment 200, 91440 Orsay, France*
[103]*Laboratório de Instrumentação e Física Experimental de Partículas - LIP, Lisboa, Portugal*
[104]*Laboratório de Instrumentação e Física Experimental de Partículas - LIP, Coimbra, Portugal*
[105]*Instituto Superior Técnico - IST, Universidade de Lisboa, Portugal*
[106]*Faculdade de Ciências - FCUL, Universidade de Lisboa, Portugal*
[107]*Lancaster University, Bailrigg, Lancaster LA1 4YB, United Kingdom*
[108]*Lawrence Berkeley National Laboratory, Berkeley, CA 94720, USA*
[109]*University of Liverpool, L69 7ZE, Liverpool, United Kingdom*
[110]*Los Alamos National Laboratory, Los Alamos, NM 87545, USA*
[111]*Louisiana State University, Baton Rouge, LA 70803, USA*
[112]*University of Lucknow, Lucknow 226007, Uttar Pradesh, India*
[113]*Madrid Autonoma University and IFT UAM/CSIC, Ciudad Universitaria de Cantoblanco 28049 Madrid, Spain*
[114]*University of Manchester, Oxford Road, Manchester M13 9PL, United Kingdom*
[115]*Massachusetts Institute of Technology, Cambridge, MA 02139, USA*
[116]*University of Michigan, Ann Arbor, MI 48109, USA*
[117]*Michigan State University, East Lansing, MI 48824, USA*
[118]*University of Minnesota Duluth, Duluth, MN 55812, USA*
[119]*University of Mississippi, P.O. Box 1848, University, MS 38677 USA*
[120]*University of New Mexico, 1919 Lomas Blvd. N.E. Albuquerque, NM 87131, USA*
[121]*H. Niewodniczański Institute of Nuclear Physics, Polish Academy of Sciences, Cracow, Poland*
[122]*Nikhef National Institute of Subatomic Physics, Science Park, Amsterdam, Netherlands*
[123]*University of North Dakota, 3501 University Ave Grand Forks, ND 58202-8357, USA*
[124]*Northern Illinois University, Department of Physics, DeKalb, Illinois 60115, USA*
[125]*Northwestern University, Evanston, Il 60208, USA*
[126]*University of Notre Dame, Notre Dame, IN 46556, USA*
[127]*Ohio State University, 191 W. Woodruff Ave. Columbus, OH 43210, USA*
[128]*Oregon State University, Corvallis, OR 97331, USA*
[129]*University of Oxford, Oxford, OX1 3RH, United Kingdom*
[130]*Pacific Northwest National Laboratory, Richland, WA 99352, USA*
[131]*Universtà Degli Studi di Padova, Dip. Fisica e Astronomia G. Galilei and INFN Sezione di Padova, I-35131 Padova, Italy*
[132]*University of Pennsylvania, Philadelphia, PA 19104, USA*
[133]*Pennsylvania State University, University Park, PA 16802, USA*
[134]*Physical Research Laboratory, Ahmedabad 380 009, India*
[135]*Università di Pisa, Theor. Division; Largo B. Pontecorvo 3, Ed. B-C, I-56127 Pisa, Italy*
[136]*University of Pittsburgh, Pittsburgh, PA 15260, USA*
[137]*Pontificia Universidad Católica del Perú, Apartado 1761, Lima, Perú*
[138]*University of Puerto Rico, Mayaguez, 00681, USA*
[139]*Punjab Agricultural University, Department of Math. Stat. & Physics, Ludhiana 141004, India*
[140]*University of Rochester, Rochester, NY 14627, USA*
[141]*Rutgers University, Piscataway, NJ, 08854, USA*
[142]*STFC Rutherford Appleton Laboratory, OX11 0QX Harwell Campus, Didcot, United Kingdom*
[143]*SLAC National Acceleratory Laboratory, Menlo Park, CA 94025, USA*
[144]*Università del Salento and Istituto Nazionale Fisica Nucleare, Via Provinciale per Arnesano, 73100 Lecce, Italy*
[145]*Universidad Sergio Arboleda, Cll 74 -14 -14, 11022 Bogotá, Colombia*
[146]*University of Sheffield, Department of Physics and Astronomy, Sheffield S3 7RH, United Kingdom*
[147]*South Dakota School of Mines and Technology, Rapid City, SD 57701, USA*
[148]*South Dakota State University, Brookings, SD 57007, USA*
[149]*University of South Carolina, Columbia, SC 29208, USA*
[150]*Southern Methodist University, Dallas, TX 75275, USA*

[151] *Stony Brook University, SUNY, Stony Brook, New York 11794, USA*
[152] *INFN - Laboratori Nazionali del Sud (LNS), Via S. Sofia 62, 95123 Catania, Italy*
[153] *University of Sussex, Brighton, BN1 9RH, United Kingdom*
[154] *Syracuse University, Syracuse, NY 13244, USA*
[155] *University of Tennessee at Knoxville, TN, 37996, USA*
[156] *Texas A&M University (Corpus Christi), Corpus Christi, TX 78412, USA*
[157] *University of Texas at Arlington, Arlington, TX 76019, USA*
[158] *University of Texas at Austin, Austin, TX 78712, USA*
[159] *Tufts University, Medford, MA 02155, USA*
[160] *University of Minnesota Twin Cities, Minneapolis, MN 55455, USA*
[161] *University College London, London, WC1E 6BT, United Kingdom*
[162] *Valley City State University, Valley City, ND 58072, USA*
[163] *Variable Energy Cyclotron Centre, 1/AF, Bidhannagar Kolkata - 700 064 West Bengal, India*
[164] *Virginia Tech, Blacksburg, VA 24060, USA*
[165] *University of Warsaw, Faculty of Physics ul. Pasteura 5 02-093 Warsaw, Poland*
[166] *University of Warwick, Coventry CV4 7AL, United Kingdom*
[167] *Wichita State University, Physics Division, Wichita, KS 67260, USA*
[168] *William and Mary, Williamsburg, VA 23187, USA*
[169] *University of Wisconsin Madison, Madison, WI 53706, USA*
[170] *Yale University, New Haven, CT 06520, USA*
[171] *Yerevan Institute for Theoretical Physics and Modeling, Halabian Str. 34, Yerevan 0036, Armenia*
[172] *York University, Physics and Astronomy Department, 4700 Keele St. Toronto M3J 1P3, Canada*

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Chapter 1

Dual-Phase Far Detector Technology

This chapter provides a brief introduction to the dual-phase far detector technology. The text below closely follows that found in the introductory chapter of Volume V, The DUNE Far Detector Dual-Phase Technology, where many more details may be found.

1.1 Overview

Deep Underground Neutrino Experiment (DUNE)'s rich physics program, with discovery potential for charge-parity symmetry violation (CPV) in the neutrino sector and its capability to make significant observations of nucleon decay and astrophysical events is enabled by the exquisite resolution of the liquid argon time-projection chamber (LArTPC) detector technique, which the dual-phase (DP) design further augments relative to the single-phase (SP) design. The operating principle of a DP LArTPC, illustrated in Figure 1.1, is very similar to that of the SP design (Figure **??**). Charged particles that traverse the active volume of the LArTPC ionize the medium while also producing scintillation light. In a DP module ionization charges drift vertically in liquid argon (LAr) and are transferred into a layer of gas above the liquid where they deposit their charge on a segmented anode. This design allows for a single, fully homogeneous LAr volume, offering a much longer drift length and reducing the quantity of nonactive materials in the LAr. While the longer drift length requires a higher voltage (up to 600 kV) on the cathode, the DP design improves the signal-to-noise (S/N) ratio in the charge readout, reducing the threshold for the smallest observable signals, while also achieving a finer readout granularity. Other advantages of the DP design include accessible readout electronics and fewer detector components, reducing costs and simplifying installation logistics. The precision tracking and calorimetry offered by the DP technology provides excellent capabilities for identifying interactions of interest while mitigating sources of background.

The argon scintillation light, at a wavelength of 127 nm, is deep in the UV spectrum. It is recorded by an array of photomultiplier tubes (PMTs) located below the cathode at the bottom of the cryostat. The PMTs, coated with a wavelength-shifting (WLS) material, shift the light closer to

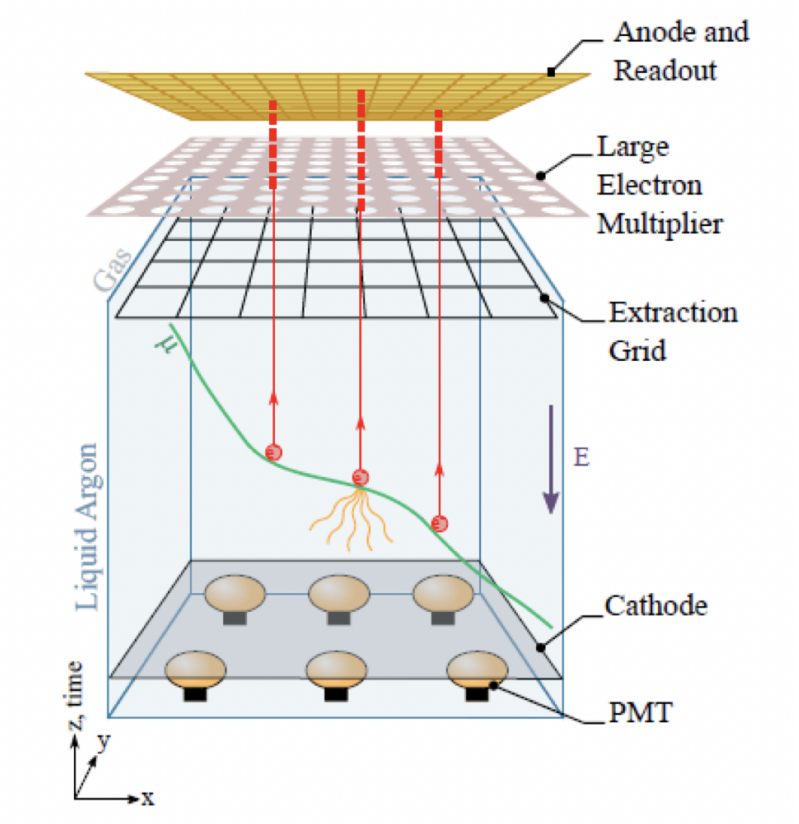


Figure 1.1: Principle of the DP readout.

the visible spectrum and record the time and pulse characteristics of the incident light.

Two of the key factors that affect the performance of a LArTPC are argon purity and noise. The DP and SP designs have slightly different purity requirements to cope optimally with the different drift lengths. We express the purity level in terms of electron lifetime: a minimum of 5 ms for DP versus 3 ms for SP. In both cases the levels of electronegative contaminants in the LAr (e.g., oxygen and water) must remain at parts per trillion (ppt) levels. To clearly discern the drifting electrons over the baseline of the electronics, the time projection chamber (TPC) electronic readout noise must be kept very low. This requires use of low-noise cryogenic electronics. Amplification of the electron signal in the gas phase mitigates the potential effect of both factors on the performance.

1.2 Features of the Dual-Phase Design

A DP module, with a 12.1 kt active mass LArTPC and dimensions (LWH) 60.0 m by 12.0 m by 12.0 m, includes all associated cryogenics, electronic readout, computing, and safety systems. The module is built as a single active volume, with the anode at the top in the gas volume, the cathode near the bottom, and an array of photon detectors (PDs) underneath the cathode. The active volume (see Figure 1.2) is surrounded by a field cage (FC). The DP design maximizes the active volume within the confines of the membrane cryostat while minimizing dead regions and the

presence of dead materials in the drift region. The detector elements are all modular to facilitate production and to allow for transport underground.

The key differentiating concept of the DP design is the amplification of the ionization signal in an "avalanche" process. Ionization electrons drift upward toward an extraction grid situated just below the liquid-vapor interface. After reaching the grid, an E field stronger than the drift field extracts the electrons from the liquid upward into the ultra-pure argon gas. Once in the gas, the electrons encounter detectors, called large electron multipliers (LEMs), that have a micro-pattern of high-field regions in which the electrons are greatly amplified (via avalanches caused by Townsend multiplication). The amplified charge is collected on an anode. The use of avalanches to amplify the charges in the gas phase increases the S/N ratio by at least a factor of ten, with the goal of achieving a gain of about 20, which will significantly improve the event reconstruction quality.

The modular extraction grids, LEMs, and anodes are assembled into three-layered sandwiches with precisely defined inter-stage distances and inter-alignment, which are then connected together horizontally into modular detection units that are 9 m^2. These composite detection units, called charge-readout planes (CRPs), are discussed in Section 1.3. A CRP provides an adjustable charge gain and two independent, orthogonal readout views, each with a pitch of 3.1 mm. It collects the charge projectively, with practically no dead region. Together, the time information (t_0) from the LAr scintillation readout and the 3D track imaging of the CRPs provide dE/dx information.

Slow-control feedthroughs, one per CRP, are used for level meter and temperature probe readout, for pulsing calibration signals, and to apply high voltage (HV) bias on the two sides of the LEMs and on the extraction grid. Calibration and cryogenic instrumentation and slow controls (CISC) systems for the SP and DP technologies have been designed jointly, and are discussed in Sections **??** and **??**, respectively.

Signals in each CRP unit are collected via three signal feedthrough chimneys (SFT chimneys) on the roof of the cryostat that house the front-end (FE) cards with the (replaceable) cryogenic ASIC amplifiers. The only active electronics elements inside the cryostat are the PMT bases. Each SFT chimney is coupled to a Micro Telecommunications Computing Architecture (μTCA) crate to provide signal digitization and data acquisition (DAQ). These crates are connected via optical fiber links to the DAQ back-end. The total number of readout channels per 10 kt module is 153,600.

Figure 1.2 shows the DP module's main components. The number of components and corresponding parameters for a 12.1 kt DP module are summarized in Table 1.1.

1.3 Charge Readout Planes

The collection, amplification, and readout components of the TPC are combined into layered modules called CRPs. The charge is collected in a finely segmented readout anode plane at the top of the gas volume and fed to the FE readout electronics. The CRP's amplification components,

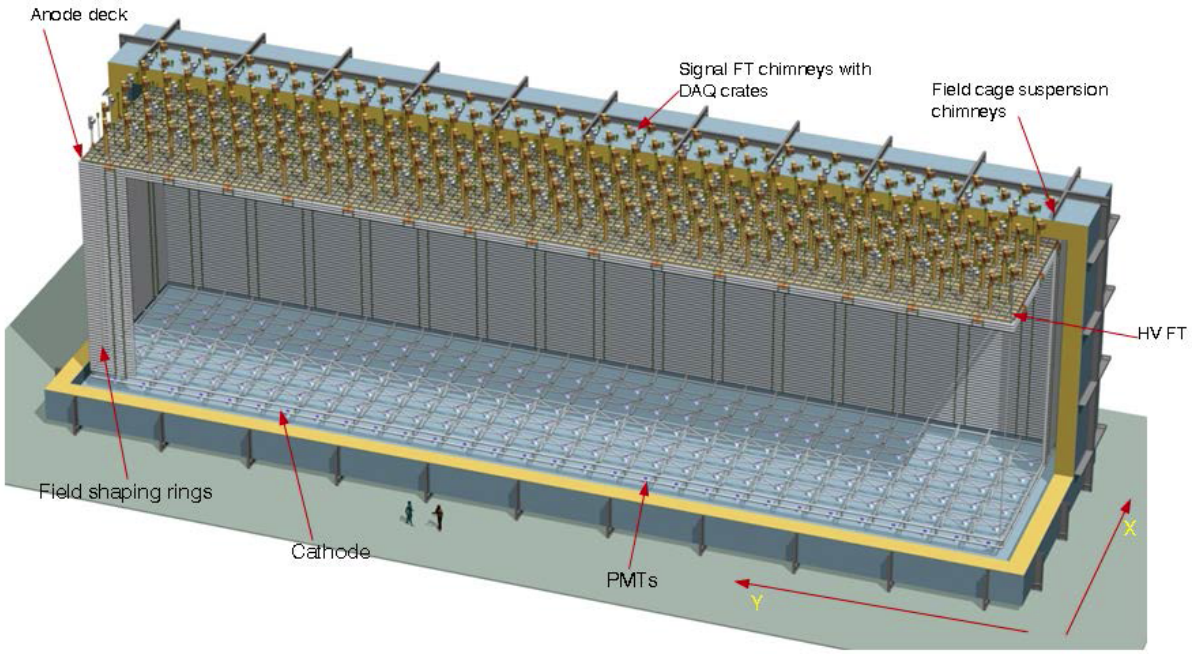


Figure 1.2: A DP module with cathode, PMTs, FC, and anode plane with SFT chimneys.

Table 1.1: DP module component quantities and parameters.

Component	Value
Anode plane size	W = 12.0 m, L = 60.0 m
CRP unit size	W = 3 m, L = 3 m
CRPs	$4 \times 20 = 80$
CRP channels	153,600
LEM-anode sandwiches per CRP unit	36
LEM-anode sandwiches (total)	2880
SFT chimneys per CRP unit	3
SFT chimneys	240
Charge readout channels per SFT chimney	640
Charge readout channels (total)	153,600
Suspension feedthrough per CRP unit	3
Suspension feedthroughs (total)	240
Slow control feedthroughs (total)	80
HV feedthrough	1
Nominal drift E field	0.5 kV/cm
Nominal/target HV for vertical drift	500 V/cm/600 kV
FC voltage degrader resistive chains	12
FC cathode modules	15
FC rings	199
FC modules (4 m×12 m)	36
PMTs	720 ($1/m^2$)
PMT channels	720

the LEMs, are horizontally oriented 1 mm-thick printed circuit boards (PCBs) with electrodes on the top and bottom surfaces. The CRP structure also integrates the immersed extraction grid, which is an array of x- and y-oriented stainless steel wires, 0.1 mm in diameter, with a 3.1 mm pitch. Figure 1.3 shows the thicknesses and possible biasing voltages for the different CRP layers.

Each CRP is made up of several independent $0.5 \times 0.5\,\mathrm{m}^2$ units, each of which is composed of a LEM-anode "sandwich." The anode is a two-dimensional (2D) PCB with two sets of 3.125 mm-pitch gold-plated copper strips that provide the x and y coordinates (and thus two views) of an event. Both the LEMs and anodes are produced in units of $50 \times 50\,\mathrm{cm}^2$. The CRPs are embedded in a mechanically reinforced frame of FR-4 and iron-nickel invar alloy.

An extraction efficiency of 100 % of the electrons from the liquid to the gas phase is achieved with an E field of the order of 2 kV/cm across the liquid-gas interface, applied between the extraction grid immersed in the liquid and charge amplification devices situated above, in the argon gas.

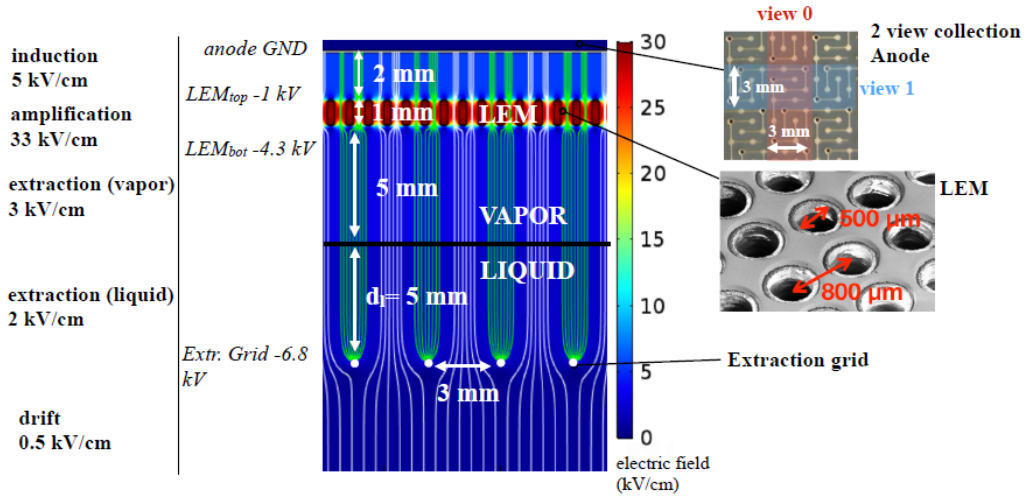


Figure 1.3: Thicknesses and HV values for electron extraction from liquid to gaseous argon, their multiplication by LEMs, and their collection on the x and y readout anode plane. The HV values are indicated for a drift field of 0.5 kV/cm in LAr.

The LEMs are drilled through with many tiny holes (these are the high-field regions), that collectively form a micro-pattern structure. When a 3 kV potential difference is applied across the a LEM's electrodes, the high E field (30 kV/cm) produces avalanches (via Townsend multiplication) that amplify the ionization electrons.

Each CRP is independently suspended by three stainless-steel ropes linked to the top deck of the cryostat. This suspension system allows adjustment of the CRP height and level such that it remains parallel to the LAr surface and the extraction grid remains immersed.

1.4 Cathode, Field Cage, and HV System

The drift field (nominal: E $\simeq$ 0.5 kV/cm, minimum: E $\simeq$ 0.25 kV/cm) inside the fully active LAr volume is produced by applying HV to the cathode plane at the bottom of the cryostat and is kept uniform by the FC, a stack of 199 equally spaced, field-shaping electrodes. These electrodes are set to linearly decreasing voltages starting from the cathode voltage at the bottom of the detector module to almost ground potential at the level of the CRP.

The cathode plane is suspended from the FC and hangs near the bottom of the cryostat. It consists of 15 adjacent 4 m $\times$ 12 m modules to span the 60.0 m length of DP module.

As shown in Figure 1.4, each cathode module is constructed of two 12 m long trusses made from thin-walled stainless steel tubes with an outer diameter of approximately 50 mm.

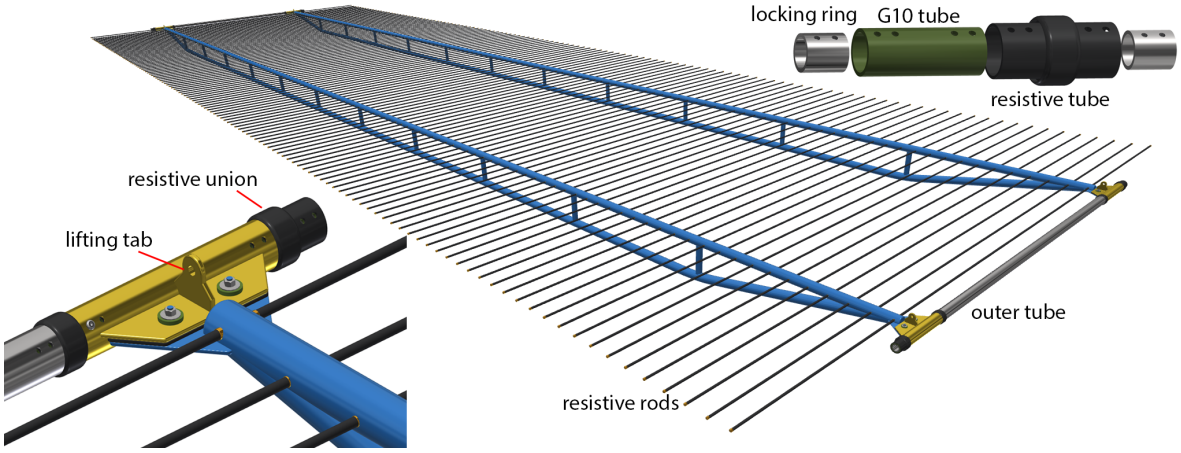


Figure 1.4: Illustration of a DP cathode module. It is constructed using a pair of stainless steel trusses (blue) as the framework with an array of coated FRP rods. The lower-left inset shows the resistive interconnections and the lifting tab on the cathode truss structure. The upper-right inset is shows the resistive union.

A set of 80 3 m $\times$ 3 m ground grid modules, standing on the cryostat floor, are installed to protect the array of PMTs against any electric discharge from the cathode.

The HV for ProtoDUNE-DP was designed for 300 kV, corresponding to a minimal requirement of E field $\simeq$0.25 kV/cm for the DP module. We can test the equivalent of a 12.0 m drift in ProtoDUNE-DP by further reducing the drift field, and in contradistinction, we expect to test the full 600 kV in a second phase of ProtoDUNE-DP after making some changes to the cathode and the HV feedthrough. Fermilab is also considering building a test setup for 600 kV operation and 12.0 m drift.

1.5 Readout Electronics and Chimneys

The electrical signals from the collected charges are passed to the outside of the cryostat via a set of dedicated SFT chimneys, tightly-fit pipes that penetrate the top layer of the cryostat insulation, and are therefore exposed to cryogenic temperatures at their lower ends and to room temperature above the cryostat. They are filled with nitrogen gas and closed at the top and bottom by ultra-high-vacuum flanges (warm and cold).

The cryogenic analog FE electronics cards, mounted on 2 m long blades that slide on lateral guides that are integrated into the mechanical structure of the SFT chimney, are installed at the bottom of the chimney and plugged into the top side of the cold flange. This arrangement allows access to and replacement of the cards from the outside. The warm flange connects the analog differential signals to external digitization cards. In the other direction, it distributes the LV and slow control signals to the FE electronics. The chimneys act also as Faraday cages, preventing the analog FE electronics from picking up possible noise from the digital electronics.

The FE cards are based on the analog cryogenic preamplifiers implemented in CMOS ASIC circuits designed for high integration and large-scale affordable production. The ASIC for the DP module circuits have been specially engineered to match the DP module's signal dynamics. Inside the SFT chimneys, the cards are actively cooled to a temperature of approximately 110 K. The bottom sides of the cold flanges connect to CRPs via flat 0.5 m long cables intended to minimize the input capacitance to the preamplifiers. Each SFT chimney collects 640 readout channels.

The digital electronics for the charge digitization system is installed on the cryostat roof. This makes it possible to use common design standards and benefit from commercially supported low-cost, high-speed networking technologies, such as μTCA, which is used in the telecommunications industry.

Digitization cards in the advanced mezzanine card (AMC) format read 64 channels per card. Each AMC card can digitize 64 channels at 2.5 MHz and compress and transmit this continuous data stream, without zero-skipping, over a network link operating at 10 Gbit/s. Lossless data compression is particularly effective thanks to the high S/N ratio of DP, which limits noise contributions at the level of one analog-to-digital converter (ADC) count. Each SFT chimney is coupled to a μTCA crate that holds 10 AMC digitization cards and can therefore read 640 channels. The AMC cards transmit the data to the DAQ back-end. A total of 240 μTCA crates are required for reading the entire detector module.

The light-readout digitization system uses μTCA AMC card design derived from that of the charge readout system, but that implements a circuitry based on the charge and time integrated readout chip (CATIROC) ASIC to trigger the readout.

The timing synchronization is based on the White Rabbit (WR) standard. Specifically developed timing MicroTCA Carrier Hub (MCH) connected to a WR network ensures the distribution of clock, absolute timing, and trigger information on the backplane of the μTCA crates. The White Rabbit μTCA Carrier Hub (WR-MCH) are connected via 1 Gbit/s optical fibers to a system of WR switches that interconnect the WR network. This ensures that the digitization performed by

the various AMC cards is completely aligned; it also refers to the absolute UTC time.

1.6 Photon Detection System

The photon detection system (PD system) is based on an array of PMTs uniformly distributed below the cathode. The PMTs have a tetra-phenyl butadiene (TPB) coating on the photocathode's external glass surface that shifts the scintillation light from deep UV to visible light. The PMTs sit on the corrugated membrane cryostat floor, on mechanical supports that do not interfere with the membrane thermal contraction. Figure 1.5 shows the PMT with its support base attached to the bottom of the ProtoDUNE-DP cryostat (Section **??**).

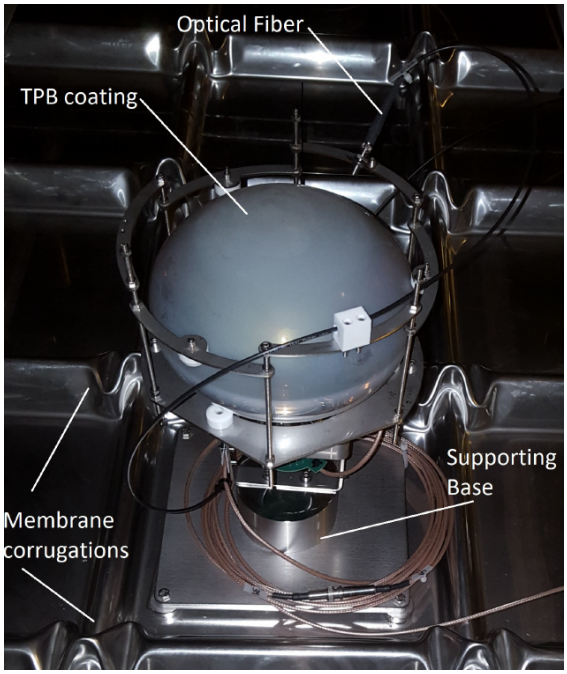


Figure 1.5: Picture of the cryogenic Hamamatsu R5912-MOD20 PMT fixed on the membrane floor of ProtoDUNE-DP. The optical fiber of the calibration system is also visible.

In order to improve the light yield uniformity for signals generated in the top part of the drift volume a system of reflective panels with WLS coating is integrated on the FC walls.

1.7 Data Acquisition

The DAQ systems for both the SP and DP technologies have been designed jointly and are identical except for the architecture of the detector readout electronics. The output format of the generated data is common, and both are synchronized to the same global clock signals. The shared DAQ design is introduced in Section **??**.

The DP readout architecture can be organized into 20 regions of interest (ROIs). Triggers are searched on the level-1 event builder machines, interconnecting multiple μTCA crates, on a sliding windows of 10 s contained in the event builder RAM. Figure 1.6 illustrates the DP readout architecture (bottom) and its interface to the DAQ system.

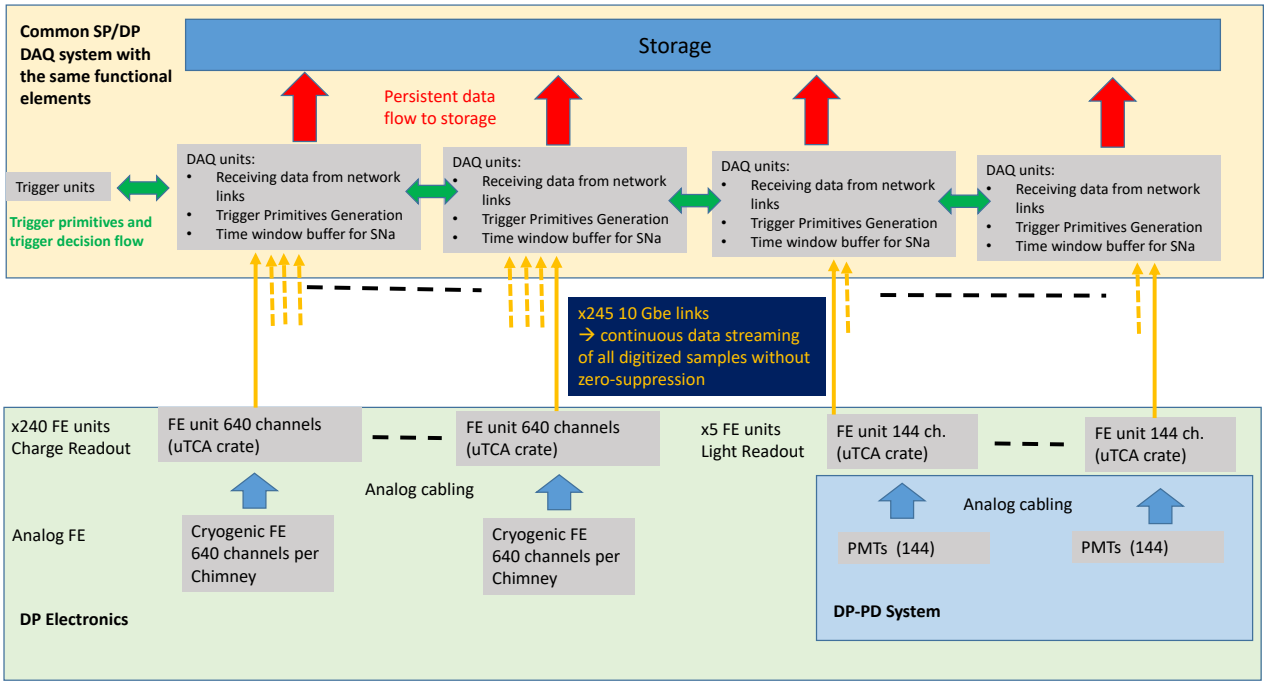


Figure 1.6: Schematic illustration of the interface of DP TPC electronics to DAQ.

References