Offline Resampling of VD ADC Waveforms

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These slides are updated to reflect discussion. Updates are in red.

Sampling as described in the VD TDR

Top Detector Electronics (TDE)

*…sampling can be performed either at **2.5 MSPS** or at **2.0 MSPS**…*
*…when operating in the **2.5 MSPS** sampling mode, data are acquired at a sampling rate a factor of **eight higher, then down-sampled** in the FPGA to **2.5 MHz**…*
*…configuration planned for **FD2-VD** operation is simpler; it is based on a **2.0 MSPS** final sampling rate, 12 bit dynamics…*
*…WRclock (**125 MHz**)…*

Bottom Detector Electronics (BDE)

*…DUNE will use a **62.5 MHz** master clock, so the digitization frequency will be **1.953 MHz** (1 / **512 ns**). For **convenience**, the digitization clock is referred to as 2 MHz and the master clock as 64 MHz.…*

Editorial: rounding of sampling numbers is not at all convenient to this human!

What are the actual, exact samplings?

Assumption: ADC sampling must be a multiple of the base clock. (Right?)

In discussion: TDE is **exact** 2.0 MSPS and the clock multiplier argument does not apply.

det half	clock (MHz)	clock (ns)	mult (×)	ADC (ns)	ADC (MHz)	TDR quote
TDE	125	8	50	400	2.5	"2.0 MSPS"
			62	496	2.016129	
			63	504	1.984127	
			64	512	1.953125	
BDE	62.5	16	25	400	2.5	"1.953 MHz"
			31	496	2.016129	
			32	512	1.953125	

Questions for detector electronics experts

(who ~~are likely not~~ were at this meeting)

TDE Which exact sampling would be chosen as “2 MSPS”?

- It is exactly 2.0 MSPS.

BDE Why choose “1/512 ns” as “2 MHz” when “1/496 ns” is closer?

- Easier to divide by 32 than 31.

both Why both TDE and BDE can not use common and “more round” 2.5 MHz?

- "2 MHz" defined by the formal DUNE requirement statements.

(Answers given in discussion.)

Problems if TDE and BDE use different sampling

- Either **same readout time** ($\approx 4\,\mathrm{ms}$) XOR **same #samples** ($N \approx 8\mathrm{k}$), **can not have both**.
- Sloppy **stitching** of 3D reco objects across top/bottom boundary.
- Need separate T/B **field response calculations** despite same CRP design.
- Complexity of two `tick` values floating around the configuration.

What can offline do help this situation?

Just as we may do online, so may we **resample** ADC waveforms in the offline.

But, we must be mindful of:

- Signal processing theory,
- Computational costs,
- Introducing more human confusion.

Nevertheless, let us consider resampling VD BDE ADC waveforms to **exactly** our old friend:

$$T = 500\,\mathrm{ns},\ F = 2\,\mathrm{MHz}$$

Signal resampling $R \equiv \frac{F'}{F} = \frac{T}{T'} = \frac{N'}{N}$

Keep total signal duration (NT) fixed.

upsampling $R > 1$ **increases** Nyquist frequency

- Nyquist/Shannon, "no worries, this is a lossless transform".
- Beware of interpolation **artifacts**.

downsampling $R < 1$ **decrease** Nyquist frequency

- Nyquist/Shannon, "if signal bandwidth $> F'_{nyquist}$ then":
  - You will cause **aliasing** unless a **low-pass filter** is applied.
  - You will lose info regardless.

Given a choice, prefer **lossless upsampling** so please make "2 MSPS" to mean:

TDE ~~1.984127 MHz (504 ns)~~ exactly 2.0 MHz (500 ns),

BDE 1.953 125 MHZ (512 ns).

Implementation issues

Want to **minimize offline exposure** to "non-2 MHz" waveforms.

- Wire-Cell **Noise Filter** is first to "touch" decoded ADC so **best home for resampling**.
- NF must already perform FFTs and so may use **frequency-space** resampling.
  - Generally more spectrally-correct than **interval-space** resampling "for free".
  - (There are many details to this topic that I skip here).
- Wire-Cell TPC drift/detector simulation, signal processing and all downstream would continue to run at 2 MHz.

Proposal

- DUNE VD BDE electronics will target $F \lesssim 2\,\mathrm{MHz}$ sampling by the ADCs.
- DUNE **offline will resample VD signals to exactly** $T = 500\,\mathrm{ns},\ F = 2\,\mathrm{MHz}$.
  - Resampling will be performed early and inside WCT Noise Filter.

Path to acceptance and implementation

- Seek broad input from DUNE collaboration.
  - Especially from VD electronics and offline experts.
- Develop the specific method.
  - An optimized software conceptual design has being developed but too many details for today.
  - Flesh out into technical note.
  - Measure computational costs of the “bare” method.
- Integrate into WCT Noise Filter.
  - Observe no measurable computational cost increase.
  - Demonstrate and validate the method on coldbox data and sim.
- Put into production.