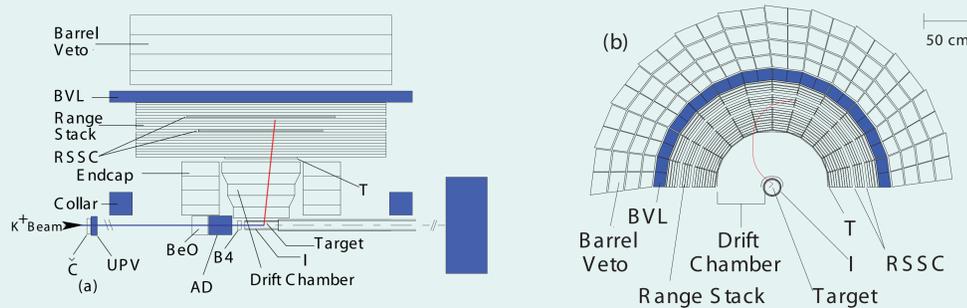


# Upgrade of the Level-0 trigger system for BNL-E949

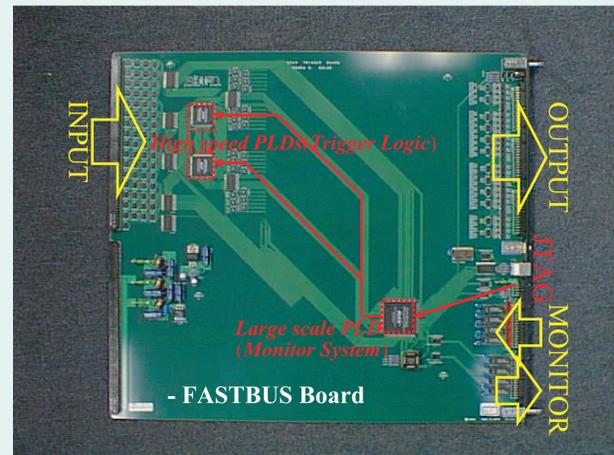
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## - The E949 Experiment

The BNL-E949 experiment, which is a successor to E787, aims to measure the branching ratio of the rare kaon decay  $\pi^+\nu\bar{\nu}$  whose branching ratio is predicted to be  $10^{-10}$ . Several improvements, one of which is the upgrade of the Level-0 trigger system, were made to E787 in order for E949 reach a sensitivity of  $10^{-11}$  and observe 10 Standard Model events.



## - Programmable Level-0 Trigger Board



The L0 trigger board for E787 used wire-wrap ECL logic in a FASTBUS board; one has to re-wire the board to modify the trigger condition. In E949, trigger modifications were expected because of the detector upgrade, and we therefore developed a new programmable L0 trigger board.

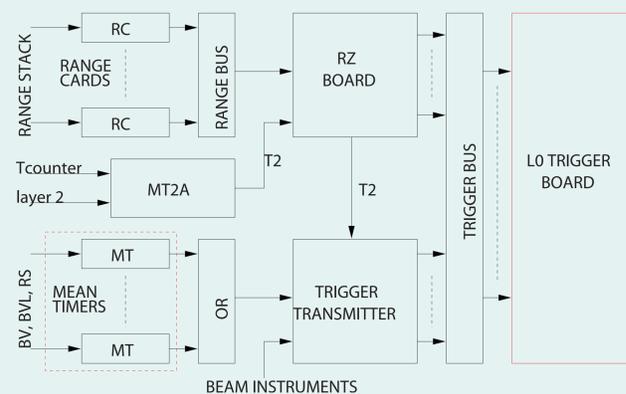
High-Speed PLD	EPM7032B-4
Large-Speed PLD	EPF10K100E-1
Board Size	FASTBUS
Input	65 ECL at back 16 ECL at front
Output	24 ECL(duplicated) 3 Or-ed 16 ECL at front

- High-speed PLD for trigger logic
- Large-scaler PLD for various applications
  - prescaler
  - scaler
  - hit pattern finder

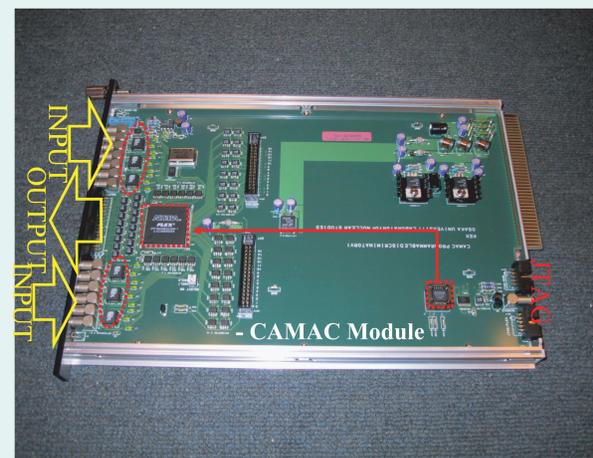
## - E949 Level-0 Trigger System

$$\pi^+\nu\bar{\nu} \equiv K_B \cdot DC \cdot (T \cdot 2) \cdot (6_{ct} + 7_{ct}) \cdot \overline{19_{ct}} \cdot RR \cdot L0\_zfrf \cdot \overline{(BV + BVL + EC)} \cdot HEX$$

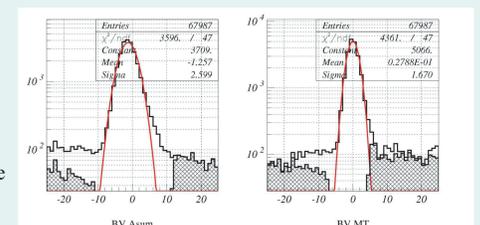
The E949 experiment aims to accumulate more statistics with higher beam intensity than E787. The trigger system must work more flexibly and with less dead time. In E949, programmable L0 trigger board installed instead of the E787 trigger board for the flexibility of the trigger. Digital Mean-timer modules were installed to reduce dead time. Both modules have Programmable Logic Device(PLD).



## - Digital Mean-timer



In E787, analog sum signals of the single end of the RS and BV counters were used for the photon veto signal, and the veto time width was large to account for the timing variations due to the z-position of the photons. By using a Mean-timer module, the veto time width can be narrowed and accidental veto rate is therefore reduced.

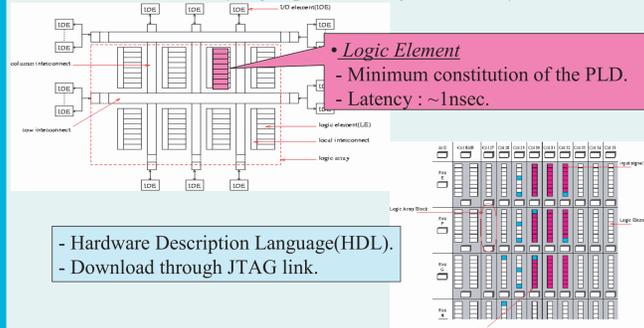


Performance of the digital Mean-timer. Left figure shows the time distribution of analog sum and right figure shows the distribution of Mean-timer. Open histogram shows  $K_{\pi^2}$  distribution of hit times in the photon veto bit is not set. Shaded histogram shows the time distribution for events with the bit set. In all cases the time distributions of the photon veto signals is shown relative to the time of the  $\pi^+$  track.

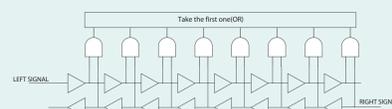
Large-Scale PLD	EPF10K50E-1
Board Size	CAMAC
Input	12 analog at front
Output	16 ECL at front

## - Programmable Logic Device (PLD)

PLDs are remarkably high-speed and large-scale today.



HDL example(Mean-timer logic)



```

FOR i IN 0 TO nmt-1 GENERATE
  m[i] = LCELL(R_delay[nmt-i-1] & L_delay[i]);
END GENERATE;

FOR j IN 0 TO (nmt DIV 4)-1 GENERATE
  mm[j] = LCELL(m[4*j+3..4*j+1] != 0);
END GENERATE;

FOR j IN 0 TO (Tw DIV 4)-1 GENERATE
  mz[j] = LCELL(m[4*j+3+Ts..4*j+1+Ts] != 0);
END GENERATE;
mz[(Tw DIV 4)] = LCELL(m[4*Tw+Ts..4*(Tw DIV 4)+Ts] != 0);
a_trig = LCELL(mm[1] != 0);
    
```

- Hardware Description Language(HDL).
- Download through JTAG link.

## - Summary

We have developed the L0 trigger board and digital Mean-timer module for the BNL-E949 experiment. The L0 trigger board allowed us rapid and simple programming of the triggers. In addition to the flexibility, the online dead time was reduced by on-chip prescaler. A powerful diagnostic capability provided quick and easy debugging of the new trigger logic. The digital Mean-timer modules were installed to reduce online dead time. Using the modules, a factor of two narrower veto width has been realized.