

Upgrade of the Level-0 Trigger System for BNL-E949

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Abstract—A new programmable trigger board and digital mean-timer modules using complex programmable logic device have been introduced to the trigger system of the BNL-E949 experiment. The online dead time was reduced from 4.0% to 1.7% by introducing an on-chip prescaler to the programmable trigger board. The acceptance loss of the online photon veto was reduced from 4.9% to 1.8% by introducing the mean-timer modules.

Index Terms—Complex programmable logic device (CPLD), field-programmable gate array (FPGA), mean-timer, trigger.

I. INTRODUCTION

THE BNL-E949 experiment [1], which is a successor to E787 [2], aims to measure the branching ratio of the rare kaon decay $K^+ \rightarrow \pi^+ \nu \bar{\nu}$ whose branching ratio is predicted to be 10^{-10} [3]. Several improvements, one of which is the upgrade of the Level-0 trigger system described here, were made to E787 in order for E949 to reach a sensitivity of 10^{-11} and observe ten standard model events.

E949 observes kaons decaying at rest. Kaons are produced by 21.5 GeV protons from the Alternating Gradient Synchrotron

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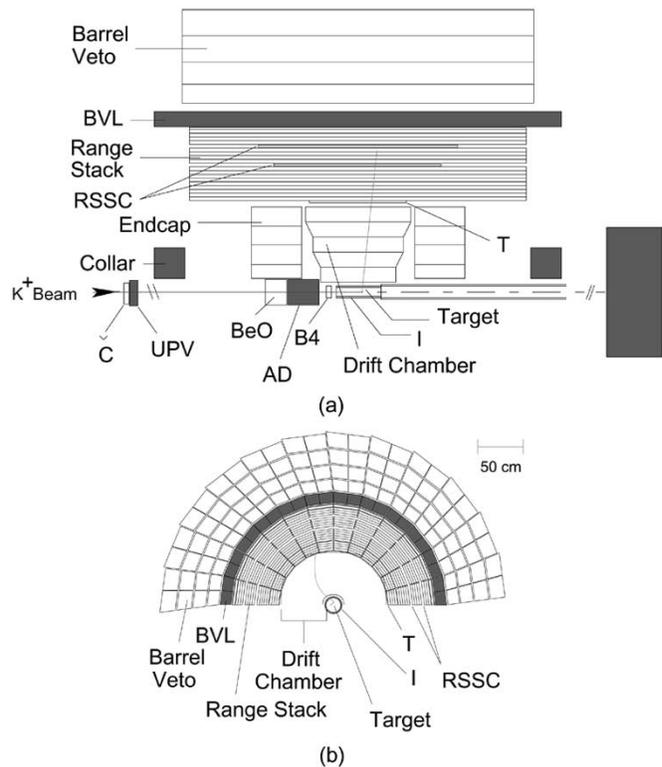


Fig. 1. (a) Schematic sideview and (b) endview of the upper half of the E949 detector. The subsystems of BVL, collar, upstream photon veto, active degrader, and downstream photon veto are newly installed for E949 (shaded parts of the figure).

(AGS) incident on a 6-cm Platinum production target. Particles produced at zero degrees are transported to the E949 detector via the low energy separated beamline 3 (LESB3) [4].

The E949 detector is shown in Fig. 1. The detector is situated in a 1-Tesla magnetic field parallel to the beam axis. An incident kaon comes to rest and decays in the target which is composed of a bundle of scintillating fibers. The momentum of charged decay products is measured with a cylindrical drift chamber [5] surrounding the target. The particles come to rest in the range stack (RS) consisting of 19 layers of plastic scintillator segmented into 24 azimuthal sectors. The pulse shapes of both ends of each RS counter are recorded by 500-MHz transient digitizers (TDs) [6] in order to observe the $\pi^+ \rightarrow \mu^+ \rightarrow e^+$ decay chain. Photon detectors cover the full 4π solid angle: the central barrel region is covered by the Barrel Veto (BV) and Barrel Veto liner (BVL), which are lead-scintillator sampling calorimeters, and the region along the beam axis is covered by endcaps of undoped-CsI (EC) [7]. The remaining gaps near the beam axis are

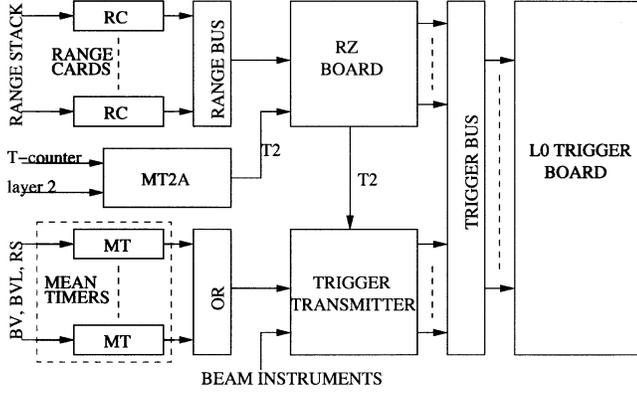


Fig. 2. A block diagram of the E949 L0 trigger system. All trigger decisions, defined as combinational logic of L0 trigger bits on the T-Bus, are performed by the L0 trigger board. Note that the dashed line region at the bottom-left corner of the figure are newly installed mean-timers described later.

covered by photon veto detectors. In particular they consist of the collar, microcollar, upstream photon veto, active degrader, and downstream photon veto.

A total of 3.5×10^6 kaons enter the E949 target in each 2.2 s spill every 5.4 s. In order to meet the data transfer speed (10 MB/s), the number of triggers per spill must be reduced. The E949 trigger system consists of fast Level-0 (L0) trigger, Level 1.1 (L1.1), and Level 1.2 (L1.2) triggers. They are based entirely on ECL signals. A block diagram of the E949 L0 trigger system is shown in Fig. 2. The L0 trigger system is composed of several FASTBUS modules. Two trigger boards (the ‘‘RZ board’’ and ‘‘Trigger Transmitter’’ in Fig. 2) latch a variety of signals from the detector onto the 65 bit wide trigger bus (T-Bus), which is then read by the L0 trigger board. The L0 trigger board makes a decision using the T-Bus bits. The L1.1 and L1.2 triggers involve processing of TD and ADC data with a longer decision time but at the lower rate of events that pass the L0 trigger.

The trigger condition for $K^+ \rightarrow \pi^+\nu\bar{\nu}$ is defined as follows:

$$\begin{aligned} \pi^+\nu\bar{\nu} \equiv & K_B \cdot DC \cdot (T \cdot 2) \\ & \cdot (6_{ct} + 7_{ct}) \cdot \overline{19_{ct}} \cdot RR \cdot \overline{L0_zfrf} \\ & \cdot (\overline{BV + BVL + EC}) \cdot HEX \\ & \cdot L1.1 \cdot L1.2 \end{aligned}$$

where K_B requires that a K^+ in the beam enters the target, and DC is the online Delayed Coincidence bit which requires that the time of the outgoing pion is at least 1.5 ns later than the time of the incoming kaon. The $T \cdot 2$ signal is a coincidence of the first and second layer of the RS in the same sector, which ensures the pion enters the RS. The trigger bit $6_{ct} + 7_{ct}$ requires that the pion reaches the sixth or seventh layer of the RS and suppresses the $K^+ \rightarrow \pi^+\pi^+\pi^-$ or $K^+ \rightarrow \pi^+\pi^0\pi^0$ backgrounds. The $\overline{19_{ct}}$ signal requires that the pion does not reach the nineteenth layer and suppresses $K^+ \rightarrow \mu^+\nu$ (called $K_{\mu 2}$) background. The ‘‘ct’’ designates the RS sectors that are associated with a $T \cdot 2$ ($T \cdot 2$ sector plus the next two clockwise sectors; this is the direction that a positive particle moves in the magnetic field). The RR bit is a refined range of the charged track calculated from the online information which rejects events with long range such as μ^+ from $K_{\mu 2}$ decay. BV + BVL, EC and HEX are online photon veto bits from the barrel region, Endcap region and RS, respectively,

TABLE I
SPECIFICATIONS OF THE L0 TRIGGER BOARD

High-speed PLD	EPM7032B-4
Large-scale PLD	EPF10K100E-1
Board Size	FASTBUS
Input	65 ECL at back 16 ECL at front
Output	24 ECL (duplicated) 3 Or-ed (output) 16 ECL at front

which remove events with photons such as $K^+ \rightarrow \pi^+\pi^0$ (called $K_{\pi 2}$) or $K^+ \rightarrow \mu^+\nu\gamma$. $L0_zfrf$ is an online fiducial cut on the z-position of the charged track.

In addition to the $\pi^+\nu\bar{\nu}$ trigger, there are monitor triggers for the purpose of calibration and normalization, and triggers for other physics modes. All triggers can be prescaled, but the $\pi^+\nu\bar{\nu}$ trigger and sometimes other physics triggers are usually not prescaled. All trigger decisions, defined as combinational logic on L0 trigger bits, are performed by the L0 trigger board. Note that all L0 trigger bits on T-Bus are latched by $T \cdot 2$ and every $T \cdot 2$ introduces a dead time of 40 ns. As will be described later, every L0 decision signal introduces a dead time of 100 ns. With a L0 pass and a subsequent L1.1 · L1.2 pass, the start signal for readout of the data is issued.

The E949 experiment aims to accumulate more statistics with higher beam intensity than E787. The trigger system must work more flexibly and with less dead time. In E949, a programmable L0 trigger board was installed to increase the flexibility of the trigger. Digital mean-timer modules were installed to reduce the acceptance loss of the online photon veto.

II. LEVEL-0 TRIGGER BOARD

The L0 trigger board for E787 used wire-wrap ECL logic in a FASTBUS board; one had to rewire the board to modify the trigger condition. In E949, trigger modifications were expected because of the detector upgrade, and we therefore developed a new programmable L0 trigger board. The board has complex programmable logic device (CPLD) chips (a product of the ALTERA corporation). Any trigger logic can be programmed using the hardware description language (HDL). The CPLD has in system program (ISP) capability. The trigger conditions can be modified through a JTAG link without extracting the board from the crate. The specifications of the new L0 trigger board are summarized in Table I; a picture of the board is shown in Fig. 3. For the trigger logic, two high-speed PLD chips (EPM7032-B-4) are used. In addition to the high-speed PLD, the board has a large-scale PLD chip (EPF10K100E-1) for various additional applications, such as trigger prescaling and on-board diagnostics, which will be described below.

The $T \cdot 2$ signal initiates the trigger process and creates a dead time of 40 ns. If a L0 condition is satisfied, the dead time must be extended for further trigger processing. This scheme is illustrated in Fig. 4. The OR-ed L0 decision signal is fed to the RZ board, which extends the $T \cdot 2$ signal via a one-shot to 100 ns. In order to realize this scheme, the propagation time of the new

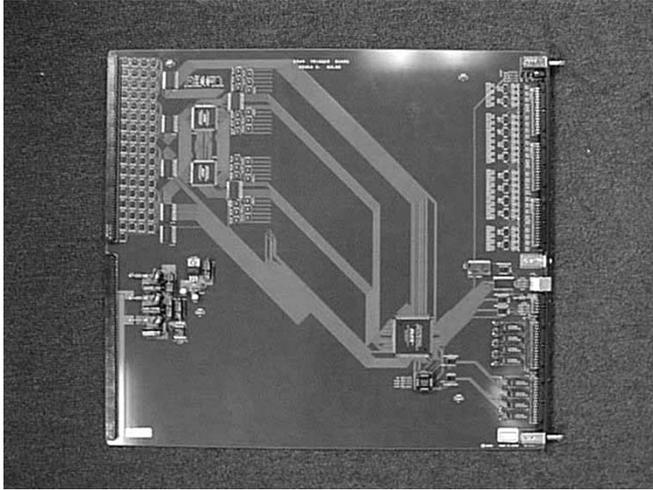


Fig. 3. A picture of the new L0 trigger board. Two high-speed PLD chips for trigger logic are located at the top-left corner. A large-scale PLD for various applications is located at the bottom-right corner.

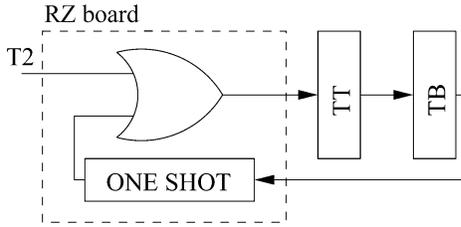


Fig. 4. A schematic view of extending the L0 dead time. Any L0 trigger decisions extend the $T \cdot 2$ width from 40 ns to 100 ns.

TABLE II
PROPAGATION TIME OF THE L0 TRIGGER BOARD

ECL/TTL + TTL/ECL conversion	2 ns
EPM7032B-4	12 ns
propagation on board	2 ns
TOTAL	16 ns

board is required to be less than 19 ns. We chose the SY100ELT24 (25) for the TTL/ECL (ECL/TTL) converter chips. The high-speed CPLD and ECL/TTL converter chips meet the requirement (see Table II).

A. Prescaler

The number of L0 decisions for monitor triggers should be prescaled at the L0 trigger board, because any L0 decision signal introduces 100 ns dead time as described in the earlier scheme. In the E787 experiment, the prescaling was done by a module after the L0 trigger board. In order to reduce the trigger dead time, it is better to prescale before the L0 decision signal of a monitor trigger is issued. We therefore introduced an on-chip prescaler to the L0 trigger board. A block diagram of the prescaler on the trigger board is shown in Fig. 5. The trigger decision signal of a monitor trigger is fed

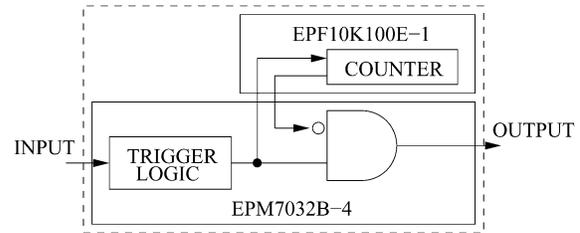


Fig. 5. A schematic view of the on-chip prescaler. After reaching the number of the prescaling factor, the large-scale PLD issues the enable signal to the high-speed PLD for the next event.

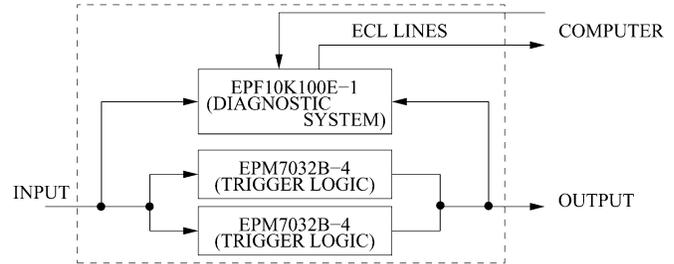


Fig. 6. A block diagram of the diagnostic system. On-chip scaler and hit pattern finder were introduced via a large-scale PLD. The information is read through ECL lines from a computer.

to the large-scale PLD, which counts the number of events. After reaching the prescale factor, the large-scale PLD issues an enable signal to the high-speed PLD for the next event. The prescaling factor can be selected through ECL lines (at front panel) from a computer. Introducing the prescaler on the trigger for monitoring the charged tracks from kaon decays (defined as $K_B \cdot DC \cdot T \cdot 2$), which required the largest prescale factor and therefore produced a dead time of 4.0%, the L0 dead time was reduced to 1.7%.

B. Diagnostic System

In the upgrade of the trigger system, debugging time is desired to be as short as possible. We therefore introduced an on-chip diagnostic system in the large-scale PLD. A block diagram of the diagnostic system is shown in Fig. 6. The large-scale PLD counts the number of events (scaler) and monitors the hit pattern of input signals from the T-Bus (hit pattern finder). The on-chip scaler counts a trigger decision signal from both new and old trigger boards, and compares the number of events. No disagreement was observed at 10^{-6} level during the engineering run of E949. A hit pattern finder allowed for easy debugging when new triggers were introduced. The information is read through ECL lines (at front panel) from a computer.

III. MEAN-TIMER MODULE

Digital mean-timer modules were installed for the online photon veto of the E949 experiment. The time distribution of the online photon veto signal due to a photon hit from a $K_{\pi 2}$ decay is peaked at around $t = 0$. This photon hit can be removed by a veto whose width is determined by the time resolution of the photon veto signal relative to that of the $T \cdot 2$.

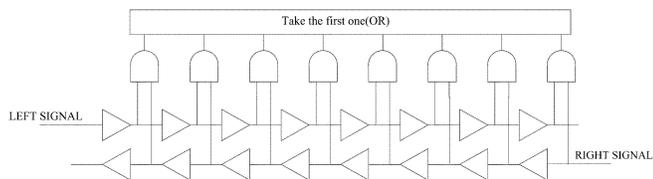


Fig. 7. Logic circuit of the digital mean-timer described in HDL. The triangles represent a logic element which is the minimum component of the CPLD (called a “delay-cell”).

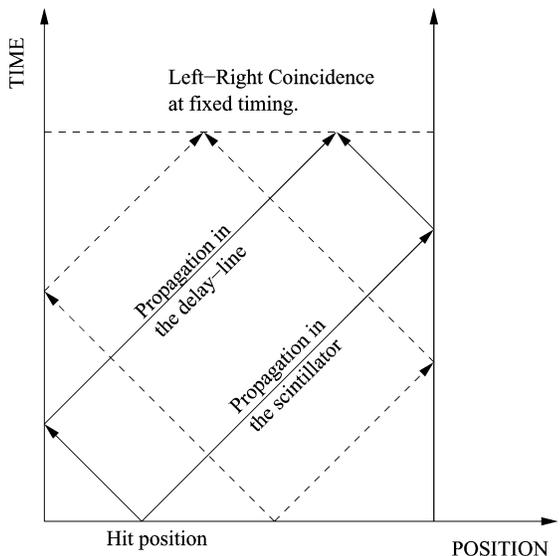


Fig. 8. Time progress of the signals in the scintillator and delay-line. Left–right coincidence for any hit positions in the scintillator (e.g., solid line and dashed line) occurs at the fixed timing.



Fig. 9. A picture of the mean-timer module. A large-scale PLD is located at middle-left of the module.

In the E787 experiment, analog sum signals of the single ends of the RS and BV¹ counters were used for the photon veto signal, and the veto time width was large (typically 20 ns) to account for the timing variations due to the z-position of the photons. By using a mean-timer module, the veto time width can be narrowed and accidental veto rate, therefore, reduced. The signals

¹Note that the BVL is new to E949 and was not in the E787 detector.

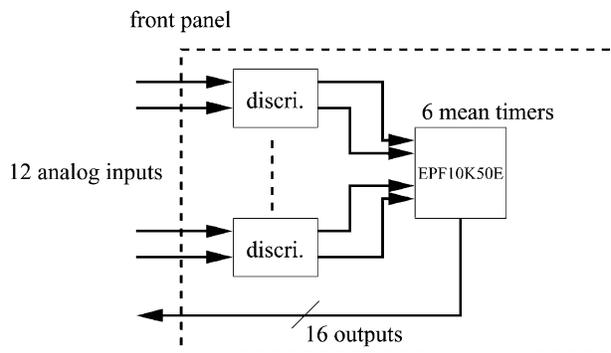


Fig. 10. A block diagram of the mean-timer module. This module combined the functions of a discriminator and a mean-timer.

TABLE III
SPECIFICATIONS OF THE MEAN-TIMER MODULE

PLD	EPF10K50E-1
Board Size	CAMAC
Input	12 analog
Output	16 ECL at front

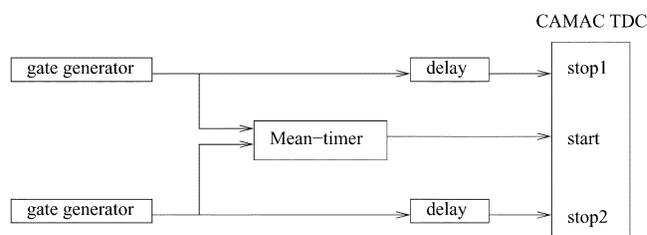


Fig. 11. A block diagram of setup for the mean-timer performance test.

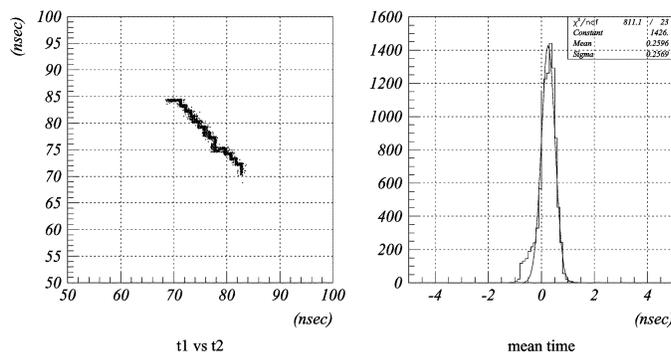


Fig. 12. Scatter plot of the two input signals (left) and difference of the online and offline mean timed signal (right). The sigma in the right plot is 0.26 ns. A dip at around $t = 78$ ns in the left plot is due to the scheme of the CPLD.

of both ends of the RS, BV, and BVL counters are mean-timed in the mean-timer. The mean-timed signals are fed to the Trigger Transmitter and used as L0 photon veto signals.

Gate arrays have been used as digital mean-timers previously [8], but we have now developed a digital mean-timer using the remarkably fast CPLDs available today. Fig. 7 shows the logic circuit of the digital mean-timer described in HDL. The triangles in the figure represent a logic element which is the minimum component of the CPLD device (called a “delay-cell”). The propagation time of the delay-cell is 1 ns [9]. The serial line of delay-cells is called a “delay-line,” and two delay-lines

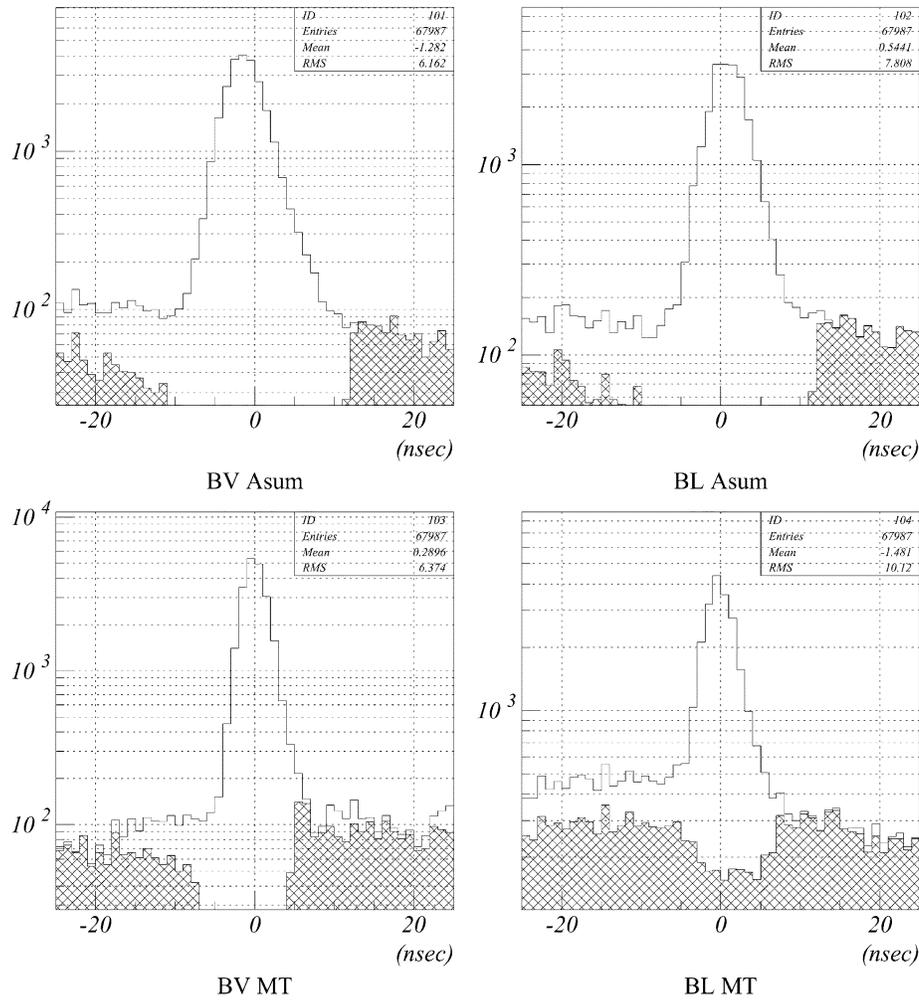


Fig. 13. Performance of the digital mean-timer. Open histogram shows K_{π^2} distribution of hit times in the photon veto systems when the bit is not set. Shaded histogram shows the time distribution for events with the bit set. In all cases the time distributions of the photon veto signals is shown relative to the time of the π^+ track.

are used in the digital mean-timer. The signal of both ends of the scintillator are fed to the delay-line. Fig. 8, shows the time progress of the signals in the scintillator and the delay-line. The left-right coincidence signals occurs at a fixed time regardless of the time difference between the left and right signals.

Due to space limitations in the electronics hut, the mean-timer combined the functions of a discriminator and a mean-timer. Six mean-timer blocks were implemented in a large scale PLD. A picture and block diagram of this module is shown in Fig. 9 and Fig. 10, respectively. The specifications are shown in Table III.

A. Performance on the Test Bench

The performance of the mean-timer was tested on a test bench. Two random signals from gate generators were input to the mean-timer module. The two input signals and the mean-timed signal were fed into a CAMAC TDC with 25 ps resolution (see Fig. 11). The left plot of Fig. 12 shows the time distribution of the two input signals. Since 12 delay-cells in a delay-line are used for this test, the range is 12 ns. The right plot of the Fig. 12 shows the time distribution of the difference of the online and offline mean-timed signals. The sigma is 0.26 ns.

B. Performance With Beam

The digital mean-timers were installed in the E949 trigger system and the performance was checked. Fig. 13 shows the time distribution of the online photon veto signal. The top-left (right) figure shows the distribution of the BV (BVL) analog sum and bottom-left (right) figure shows the distribution of the BV (BVL) mean-timer signals relative to the π^+ track time in K_{π^2} decays. The hits at around $t = 0$ due to electromagnetic showers in the detector were removed efficiently with half the veto width of the previous system. The acceptance loss of the online photon veto was reduced from 4.9% to 1.8% by introducing the mean-timer modules.

IV. CONCLUSION

We have developed a L0 trigger board and digital mean-timer module for the BNL-E949 experiment. The L0 trigger board allowed rapid and simple programming of the triggers. In addition to this added flexibility, the online dead time was reduced from 4.0% to 1.7% by introducing an on-chip prescaler to the L0 trigger board. A powerful diagnostic capability provided quick and easy debugging of new trigger logic. The digital mean-timer

modules were installed to reduce the acceptance loss of the on-line photon veto. Using these modules, a factor of two narrower veto width has been realized. The acceptance loss of the online photon veto was reduced from 4.9% to 1.8%.

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